Mark A. Indovina

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Biographical Summary

Mark A. Indovina earned his AS in applied science, and also his BS and MS in electrical engineering from Rochester Institute of Technology. He is a senior member of the IEEE (Institute of Electrical and Electronics Engineers) and AES (Audio Engineering Society). Mark is the co-author of an eBook on IC design and has authored and co-authored various technical papers, position papers, trade journal publications, and chaired and presented at society and industry forums. He has also participated in various standards bodies and committees. Most recently Mark is the Chief Operating Office of Tenrehte Technologies, a high tech, clean technology startup. Mark is also currently an adjunct professor in the Electrical & Microelectronic Engineering Department at Rochester Institute of Technology. Prior to Tenrehte, Mark was the Chief Technology Officer for Vivace Semiconductor, a high tech start-up fabless semiconductor company focused on providing digital solutions in the growing digital entertainment markets. Previously Mark was first Vice President of Engineering and then Chief Technology Officer for Improv Systems, Inc., a company which licenses intellectual property for digital signal processing including the DSP architecture, leading edge software development tools, and application packages to various markets worldwide. He has also funded directed research at local universities in topics of interest to Improv Systems. Prior to joining Improv Systems, Mark was the Director of Engineering for the Digital IC Design Group of Cadence Design Systems, where in less than 4 years he built a group of over 200 engineers performing over $65M of contract IC design for various companies throughout the world. Before Cadence Design Systems, Mark spent over 5 years in the Applied Research department of Motorola working on strategic semiconductor devices and "systems on chips" that paved the way for exciting new wireless, battery powered communications devices. During this time Mark was an adjunct professor at Florida Atlantic University where he taught classes in VLSI design, logic design, and computer architecture. He was active in obtaining NSF grants for projects assigned to the university, and joint projects partially funded by Motorola. Mark also worked with major EDA vendors to have design tools donated to the University. Prior to Motorola, Mark spent 9 years at Computer Consoles researching and developing various digital signaling processing based sub-systems as part of a novel digital switch architecture. He started his engineering career at Ashly Audio designing various products used in professional sound reinforcement. As a notable achievement, many of the products developed by Mark over the years are still in of production today. He is also the recipient of a

Philips "First Silicon" prize, an award for delivering the largest chip built to date that worked "first time" without any errors.

As an alumni advisor, Mark provides assistance to a student teams at RIT working on senior projects. An interesting example is project METEOR. METEOR is a hands-on, multi-phase, multi-disciplinary, teaching and research program for investigation and developing micro-systems engineering, science, and technologies for the exploration of outer space. The projects short-term goal is to launch small payloads into low earth orbit; the long-term goal is to place small payloads on near earth asteroids and lunar surfaces. He also is an active participant on the RIT Industrial Advisory Boards for the Electrical Engineering Department and also the Multidisciplinary Senior Design (MSD) program.

Experience

Tenrehte Technologies, Inc.   Rochester, NY

12/2008 – Present, Chief Operating Officer (COO), Founder

Tenrehte develops technologies, award winning products and initiatives to continually advance energy efficiency and reduce energy waste of any electric device that is a part of your daily life. Responsible for the day to day operations of the company; also lead product architecture, implementation, and manage the delivery of leading edge products that provide a market leading combination of high-performance, low power consumption, and superior applications flexibility. Our first product, PICOwatt®, is an award winning, Best of CES 2010 in the Green Technology Category, patented wireless smart plug designed to save you money by monitoring and reducing energy waste from any electric device.

Rochester Institute of Technology   Rochester, NY

11/2012 - Present, Adjunct Professor, Department of Electrical & Microelectronic Engineering

Responsible for preparing and presenting undergraduate, and graduate level courses covering various topics relating to analog circuits, digital circuit design, logic design, computer architecture, semiconductors, and general electrical engineering system design and implementation.

Vivace Semiconductor, Inc.   **Rochester, NY**

12/2005 – 2/2009, Chief Technology Officer (CTO), Founder

Responsible for the architecture, implementation, and delivery of cutting edge media processing SoC integrated circuits designed to address the needs of next generation consumer electronic products. The chips support multiple video compression standards including H.264/MPEG-4 AVC, MPEG-4 ASP, Windows Media Video including VC-1, MPEG-2, China's AVS, and Real Video, multiple audio compression standards such as AAC, Windows Media Audio, Real Audio, and multiple encryption standards supporting DRM including AES, DES, 3-DES and RC4.

- Started the Rochester R&D center.
- Grew organization as necessary in multiple locations including contracted services as necessary.
- Responsible for group-operating budget.
- Led architect for flagship IC projects implemented in 130, 90, and 65 nm technologies:
    - VSP-100 – 130nm, QVGA Media Platform, OpenRISC OR1200, Linux 2.6 Kernel
    - VSP-200 – 90nm, D1 NTSC/PAL Media Platform, ARM 926EJS, Linux 2.6 Kernel
    - VSP-300 – 65nm, 1080p Media Platform, ARM ARM1176JZF-S, Linux 2.6 Kernel
- Establish and manage relationships with various IP, fabless ASIC, manufacturing, and contract service providers worldwide. Responsibilities include technical and business due diligence; contract, statement of work, and cost negotiations; and execution oversight.
- Develop and maintain overall engineering goals, and product road map. Responsible for publishing methodology guides, architectural specifications, functional requirements documents, and various proposals for new development activities.
- Oversight of on going, day-to-day engineering management including budgetary planning, operations reviews, and detailed technical reviews at various levels.
- Prepare initial materials for patent attorneys for various patent submissions.
- Prepare and present project planning, cost and schedule estimates, and project engineering overview for potential internal and external customer projects.
- Assist in development of new client relationships. Create general and target specific technical presentations and deliver at customer engineering or executive level meetings.

- Develop various HR related policies and materials such as review forms and procedures, staff developments plans, engineering grade guidelines, 'ranking & rating' criteria, compensation and vacation plans.

[Improv Systems](), Inc.   Rochester, NY

2/2003 – 2/2006, Chief Technology Officer (CTO)

2/1999 – 2/2003, Vice President of Engineering

Responsible for an engineering organization charged with research and development of the VLIW based Jazz DSP, Jazz DSP Software and HW development tools, application solutions kits (Voice over IP, Multimedia, and Wireless communication), Jazz Peripherals, Jazz based standalone, SoC integrated circuits and FPGA based reference platforms used to demonstrate Improv's proprietary PSA architecture.

- Started the Rochester R&D center.
- Grew organization as necessary in 3 facilities including contracted services as necessary.
- Responsible for group-operating budget.
- Development of new client relationships. Create general and target specific technical presentations and deliver at customer engineering or executive level meetings.
- Develop and maintain overall engineering goals, and product road map. Responsible for publishing methodology guides, architectural specifications, functional requirements documents, and various proposals for new development activities.
- Day-to-day on going engineering management including budgetary planning, operations reviews, and detailed technical reviews at various levels.
- Prepare and present project planning, cost and schedule estimates, and project engineering overview for potential internal and external customer projects.
- Lead delivery of generic and customer specific application solution kits
  - Voice over IP (VoIP)
    - Includes various hardware platforms, application-optimized DSP accelerators, and supporting DSP software configurations:
      - Speech CODECs: G.711, G.722, G.723.1, G.726, G.728(i), G.729B/G.729AB, G.729A, G.729, GSM-Adaptive Multi Rate (AMR), AMR-WB, AMR-NB, CDMA Selectable Mode Vocoder (SMV)
      - Echo cancellers: G.165, G.168
      - Tone Detection and Generation, VAD, AGC, CID, multi-channel management
      - DSP Telecom Resource manager
    - Host software:
      - DSP Application Programming Interface (API)
      - Low-level driver

- Protocol stack development and integration:
  - Real-time Transport Protocol and Real-time Control Protocol (RTP and RTCP)
  - Media Gateway Control Protocol (MGCP)
  - Signaling protocols SIP or H.323
  - Multi-Media for mobile, broadcast and streaming data
    - Includes various hardware platforms, application-optimized DSP accelerators, and supporting DSP software configurations:
      - Video CODECs: MPEG-2, MPEG-4, H.264, Windows Media 9
      - Audio CODECs: MPL12, MP3, Windows Media 9
      - Audio Decoders: Dolby Digital, Prologic and AAC
      - JPEG and JPEG-2000 CODECs
      - DSP Media Resource manager
    - Host software
      - DSP Application Programming Interface (API)
      - Low-level driver
  - Wired and Wireless data-pumps
    - Includes various hardware platforms, application-optimized DSP accelerators, and DSP software blocks for technologies such as DSL, 802.11a/b/g, Turbocoding, Hyperlan, HomePlug
- Responsible for customer support for Jazz DSP development tools, hardware architecture, DSP software, and systems design. Projects implemented in 0.18, 0.15, 0.13 µm technologies
- Principle author of patent application #20010025363 "Designer configurable multi-processor system". Numerous other patent submissions.
- Develop various HR related policies and materials such as review forms and procedures, staff developments plans, engineering grade guidelines, 'ranking & rating' criteria, compensation and vacation plans.

74ze Engineering   Littleton, MA

9/2004 - Present, Advisor

Work with 74ze to review growth strategies, assess new opportunities, coach and mentor.

Cadence Design Systems, Inc.   Rochester, NY

10/1995 - 2/1999, Director of Engineering

Responsible for an engineering organization charged with research and development of turnkey integrated circuits, systems, software and tools for

customers on a contract basis. Projects scope involves complete or partial design responsibility from specification to GDSII tape-out. Activities included:

- Started the Rochester Design Center. Grew the Rochester center to 24 engineers in less than 2 years. Also started satellite centers in Orlando, FL (6 engineers) and Chelmsford, MA (10 engineers).
- P&L responsibility for the entire Digital IC Design Group.
    - Responsible for a $28M group-operating budget.
    - Responsible for managing costs to ensure revenue generation of at least $65M.
    - Grew the team to 220 associates in 6 design centers across the United States and Japan. Also developed sub-contract relationships with service firms that added an additional 120 engineers as necessary.
    - Developed and rolled out key management initiatives including Design Technology, Intellectual Property, Quality, and Associate Development.
- On going project management including internal operations reviews, technical reviews, and various project related customer meetings, including executive level presentations.
- Development of new client relationships, including project planning, cost and schedule estimates, and engineering approach for potential IC projects resulting in over $30M of bookings.
- Technical lead engineer for various IC projects, project examples include:
    - 2.5 ASIC's for an approximate total of 2M Gates; chips provided SAR and ABR functions in the data-flow path of a large capacity ATM switch. The target technology is 0.18 µm, with a maximum operating frequency of 183 MHz. Team size ranged from 18 to 40 engineer's peak. Deliverables include architecture, VHDL RTL, Verilog netlist, verification environment, parametric test vectors, and floorplans and initial placement..
    - 3 ASIC's for a total of 1M gates; chips are part of a non-linear, real time digital video editing system. The target technology is 0.25 µm, with a maximum operating frequency of 120 MHz. Team size ranged from 10 to 20 engineers peak. Deliverables include architecture, Verilog RTL, Verilog netlist, verification environment, and parametric test vectors.
    - 1 Semi-custom chip, 1M gates; this chip is a multiprocessor design with two TMS320C50 like DSP cores, and one custom 32 bit RISC, 40 peripherals. The target technology is 0.35 µm, with a maximum operating frequency of 90 MHz. Team size ranged from 24 to 60 engineer's peak. Deliverables include architecture, Verilog RTL, Verilog netlist, verification environment, CDL netlist, GDSII, parametric test vectors, production test environment, and tester probe card.

- 1 Semi-custom mixed signal (Spectre/Verilog-XL), LCD display controller/ driver chip. Team size ranged from 6 to 8 engineers peak. The target technology is 0.25μm, with a maximum operating frequency of 87 MHz. Deliverables include architecture, CDL netlist, GDSII, parametric test vectors, production test environment, and tester probe card.

- Technical lead engineer for the development of a fully synthesizable, 8 & 16-bit RISC CPU's, along with software development tools such as the assembler, linker, dis-assembler.

- Technical lead engineer for the development of a fully synthesizable, Harvard architecture, 16-bit Digital Signal Processor, along with software development tools such as the assembler, linker, dis-assembler. A cycle accurate PLI simulation model with user-defined timing of the core was also created.

- Co-authored "A Top-Down Approach to IC Design", a book focusing on leading-edge IC design practices and methods. This book complements a class in top-down described below.

- Development of the lecture and labs for a 4-week course on the topic of "Language Based Design" (often referred to as Top Down Design). The class centers on the design of single chip, a DTMF Receiver Module, and the students will perform various IC engineering tasks throughout the course modules. The course stops at the point where the chip could enter place and route, and resumes with back-annotation of delays and capacitive load files available after physical extraction. Since the design database included a custom DSP, the students are introduced to various techniques for hardware-software partitioning, design, and verification. I personally presented the class to over 150 engineers worldwide; student response was always extremely positive.

- Authored the design specification that drove development of the design center IC design environment; note that the environment is a mixture of commercial, custom, internally developed, and shareware software. Also periodically installed and configured commercial software.

- Authored the design specification that drove development of the groups' internal WEB site. This includes creation of various complex CGI interfaces for project management, bug tracking, associate skill and training databases, and site security.

Motorola   Boynton Beach, FL

2/1991 - 10/1995, Principal Staff Engineer

Member of the Applied Research - Advanced IC Technology Laboratory. Responsible for research and development of integrated circuits, and top-down design methodologies used in low-power, low-voltage, and battery powered wireless products. Numerous (un-awarded) patent submissions. Activities included:

- Development of a 900MHz digital receiver module for a "next generation" communications device. Responsible for efficient implementation of required algorithmic data processing.
- Development of a software utility which reads a Z-domain structural [Analogy Saber] netlist and creates a parallel data path or bit-serial linear difference equation implementation of the DSP algorithm in a combination of structural and fully synthesizable RTL Verilog HDL.
- Technical lead engineer for the development of parameterized macro cells which can be used as VLSI/ LSI/ MSI building blocks. Also developed a companion Cadence DFII skill application through which users can quickly develop a block implementation of their synthesizable design using the mixed text and graphics entry tool Composer. Users select the parameterized components from a palette library. The skill utility first expands the design parameters and generates Verilog HDL for module. Once code generation is complete, the utility creates and installs the module symbol and RTL Verilog HDL within the design library.
- Technical lead engineer for the modeling, characterization, and extraction for a new, "low-power", 0.5µm standard cell library for single AAA battery communications applications. Also responsible for synthesis library generation (Cadence Synergy, Synopsys Design Compiler), simulation and intrinsic timing accurate Verilog model library, Cadence CDC timing views, and library timing verification. Also assisted with cell design and layout.
- Developed an internal training course titled: "Top-Down Design with Verilog HDL". Course topics included: Verilog HDL language semantics, Verilog HDL simulation and debug, module verification techniques, Verilog HDL Language semantics for logic synthesis, mixed design entry using Cadence Composer, and a brief introduction to Mixed-Mode (Saber & Verilog-XL) simulation.
- Technical lead engineer for the development of a [custom LCD display processor IC](#) (with a final size of 4.5 million transistors including image RAM and analog blocks in 0.5 µm) utilizing top-down design techniques. Logic blocks in the design were captured in Verilog HDL and were subsequently synthesized into the Xilinx XC4k FPGA family for emulation/ verification and finally to a custom standard cell library. All hand packed custom portions of the design were behaviorally modeled in Verilog HDL. Also developed a full functional model of the device in C using the Verilog Programming Language Interface (PLI) for simulation acceleration and IP protection; the PLI model has user defined timing. A reduced resolution version of the algorithm was also implemented in silicon. Both devices were first pass successes.
- Technical lead engineer for the development of a [PCMCIA 16-bit bus interface ASIC](#) for the NewsCard data pager. The design was captured in Verilog HDL and subsequently synthesized to both the Actel ACT2 FPGA library for quick prototype and then to the Motorola 0.8µm CMOS gate array library for product implementation.

- Technical lead engineer for the development of a [PCMCIA 8-bit bus interface ASIC](#) for the NewsStream data pager. The design was captured in Verilog HDL and subsequently synthesized to both the Actel ACT2 FPGA library for quick prototype and then to the Atmel 0.8μm CMOS gate array library for product implementation.
- Technical lead engineer for the development of voice mail application software for the Digital Input/ Output Paging Processor (DIOP) based paging terminal. This project required creation of software components for both "integrated voice mail" and "call pass-through and management" to an external voice mail platform. Responsibilities included development of DSP algorithms for tone detection and generation, silence discrimination, and speech compression/ expansion; development of call scenarios and creation of call processing framework for both the "integrated" and "pass-through" voice mail applications. Also acting group leader, managing the activities of 2 applications software engineers and 3 DSP software engineers. The target hardware is MC68K based running VRTX operating system from Ready Systems.
- Development of software tools in C for UNIX workstations to simulate DSP algorithm performance. Also developed a limited operating systems for the DSP 56K and utilities for creation of various PCM test files used during algorithm acceptance testing.
- Technical lead engineer for the development of the DIOP [Voice Controller Board (VCB)](#). The VCB is a sophisticated platform for simultaneous PCM record & playback on 32 full duplex, 64 Kb/s TDM time-slots. The design contains a 33 MHz 68030 (or MC68020) with 16M byte of high performance DRAM for host application software, a 27MHz DSP56001 for PCM data processing, a 16 MHz MC68302 for high speed serial I/O, an Ethernet interface for IP communications, a SCSI bus interface for disk and tape I/O, and 8M byte of tri-ported, interleaved high performance DRAM for shared file I/O storage. The design form-factor is 9U VME with a proprietary digital switching backplane interface. Because of component density and schedule constraints, extensive use of quick turn gate array ASIC, and FPGA technology was required for enhanced functionality and increased reliability. This portion of the design was created using Verilog HDL, simulation and synthesis. Also performed full-functional simulation of the card, including porting of the real-time operating system kernel and development of board level diagnostics within the simulation environment.
- Provided technical leadership to junior engineers designing line interface circuits. Analog interfaces included loop-start, ground-start, reverse battery, and 2/ 4 wire E&M. Digital interfaces included T1 D4, T1 ESF, E1 CASD, T1 Primary Rate ISDN, and E1 Primary Rate ISDN.
- Also active in obtaining NSF grants for projects at Florida Atlantic University that were partially funded by Motorola.

[Florida Atlantic University](#)   Boca Raton, FL

1/1994 - 12/1995, Adjunct Professor

Responsible for preparing and presenting graduate level courses covering various topics relating to logic design, computer architecture, and semiconductors, VLSI, Verilog HDL, and VHDL. During this time I was very active in obtaining NSF grants for projects exclusive to the university, and joint projects partially funded by Motorola. I also worked with major EDA vendors to have design tools donated to the University.

Afghan Dog Software   Boynton Beach, FL; Rochester, NY

2/1993 - Present, Chief Engineer

Develop share-ware utilities for use with Verilog HDL, Linux, Apache. Activities include:

- Development of a fully synthesizable DSP (called the TDSP) along with various software development tools (assembly level only). The TDSP is a 16-bit, fixed-point general-purpose DSP core. The core is designed for low power, low voltage and high-speed DSP applications.
- Development of a linear timing model delay calculator/ back-annotator. This program is written in C using the Verilog Programming Language Interface (PLI). The application is capable of estimating capacitive loads modeled using a linear interpolation algorithm; the program can also estimate capacitive loads using a supplied wire technology file for wire load and wire delay calculation.
- Development of a fully automated technology library translator. This program translates a Synopsys Design Compiler technology library into a Verilog HDL source gate level, timing accurate simulation library compatible with the PLI delay calculator. The resulting Verilog technology library is also suitable as a source library for the Synergy logic synthesis tools from Cadence Design Systems.

[Computer Consoles,](#) Inc.   Rochester, NY

7/1982 - 2/1991, Sr. Engineering Specialist

Member of the Voice & Switching Products Group. Responsibilities included research and development of DSP algorithms and systems for tone detection, tone generation, silence discrimination, speech compression/ expansion, adaptive gain control, adaptive echo cancellation, speaker independent speech recognition, and test-to-speech. Created various tools and simulators using C within the UNIX environment for development of DSP algorithms. All DSP hardware and application firmware was tightly controlled as one project for maximum real-time performance for the least cost. All designs were "full-functional" simulated. Activities included:

- Introduction of digital signal processing (DSP) to CCI products by developing replacement for analog tone signaling circuit pack. Initial TMS32010 based design save $8k per circuit pack; realized over $1.2M direct savings (profit) during the first 6 months of production.
- Developed second generation (TMS320C25 based) and third generation (TMS320C30 based) tone signaling circuit pack hardware and firmware. Each module is capable of processing 32 simultaneous calls.
- Developed speaker independent, multi-lingual, isolated word, speech recognition circuit pack hardware and firmware. Each module is capable of processing 16 simultaneous calls with over 160 words in the active vocabulary.
- Prototype development of a large vocabulary, including proper names, test-to-speech circuit pack hardware and firmware.
- Developed T1 digital trunk interface circuit packs, both hardware and firmware.
- Participated in development of a third and forth generation, fully digital Audio Response (PCM record & playback) Subsystems. Assisted in the analog design portion of the first and second-generation subsystems.
- Assisted in development of a high stability clock synchronization circuit pack.
- Assisted in development of analog trunk circuit packs.
- Participated in development of a high performance, primary rate ISDN communication subsystem for a proprietary, fault-tolerant, real-time UNIX super-minicomputer. This subsystem was capable of supporting LAPB, X.25, LAPD, and Signaling System No. 7 peer-to-peer communication simultaneously on 24, 64 Kb/s TDM time-slots.
- Member of a team which ported digital switch application & call-processing software to a virtual memory compute platform. Additional responsibilities included cache memory and translation characterization and optimization for maximum transaction performance.
- Developed instruction/ data cache logic for 32-bit, virtual memory CPU.
- Attended telecommunications (Committee T1) standard committee meetings as a voting member.

Ashly Audio, Inc. Rochester, NY

6/1979 - 7/1982, Engineer

Responsible for the research and development of professional audio products. Also provided manufacturing and customer support for entire product line. Certain designs were modeled with the UCB Spice simulator. Activities included:

- Power Amplifier product line (100Wx2, 250Wx2) utilizing fully discrete and complimentary transistor topology. Amps had power MOS-FET output stages.
- State variable, 18-dB/octave active crossover product line.

- State variable notch filter incorporating a novel positive feedback circuit utilized during set up for optimum feedback control.
- Audio spectrum analyzer capable of being displayed on an inexpensive television set.

Ashly Audio, Inc.   Rochester, NY

6/1977 - 6/1979, Test Engineer

Performed circuit card, sub-assembly, and finished product test procedures using proprietary computed test bed (DRONE). Developed test procedures, test programs, additional DRONE subsystems to extend functionality, and access fixtures required for new products or for enhanced system test functionality.

Education

[Rochester Institute of Technology](#)   **Rochester, NY**

Master of Science in Electrical Engineering 1987

- o Concentration:
    - Signal Processing
    - Integrated Circuit (IC) Design
- o Thesis: *"A digital Signal processing Based Tone Receiver"*

Bachelor of Science in Electrical Engineering 1982

- o Deans List

Associate of Applied Science 1979

Senior member of the IEEE (Institute of Electrical and Electronics Engineers)

Member AES (Audio Engineering Society)

Patents

#GB2499164 [Appliance network connectivity apparatus](#) (2017)

#US09438492 [Self-Organized Multiple Appliance Network Connectivity Apparatus](#) (2016)

#US09197949 [Self-Organizing Multiple Appliance Network Connectivity Apparatus For Controlling Plurality Of Appliances](#) (2015)

#US20120143387 [Appliance Network Connectivity Apparatus](#) (2012)

#US20010025363 [Designer Configurable Multi-Processor System](#) (2001)

[PDF](#)